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Weak link detection in memory periphery using PrimeSim™ Design Robustness (DR)

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Agenda

- Motivation
- Existing statistical analysis methods and limitations
- Primesim Design Robustness (DR) flow
- Running DR on single port SRAM
- Result analysis
- Summary

Diversified application domains @ST with intensive usage of memory

Dedicated Automotive ICs

Analog, Industrial & Power Conversion ICs

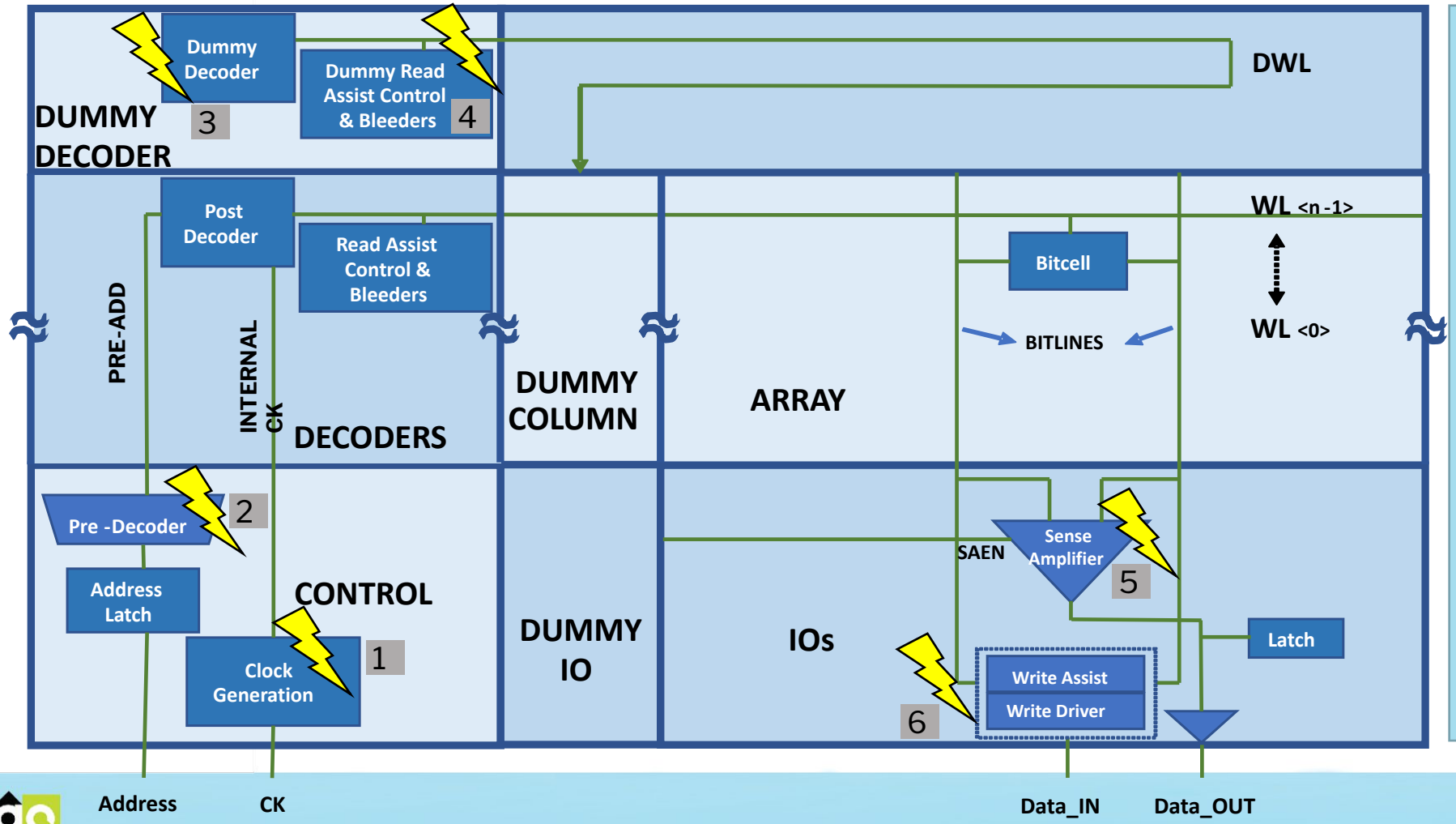
GP MCU & MPU, Secure MCUs, EEPROM

Discrete & Power Transistors

MEMS & Optical sensing solutions

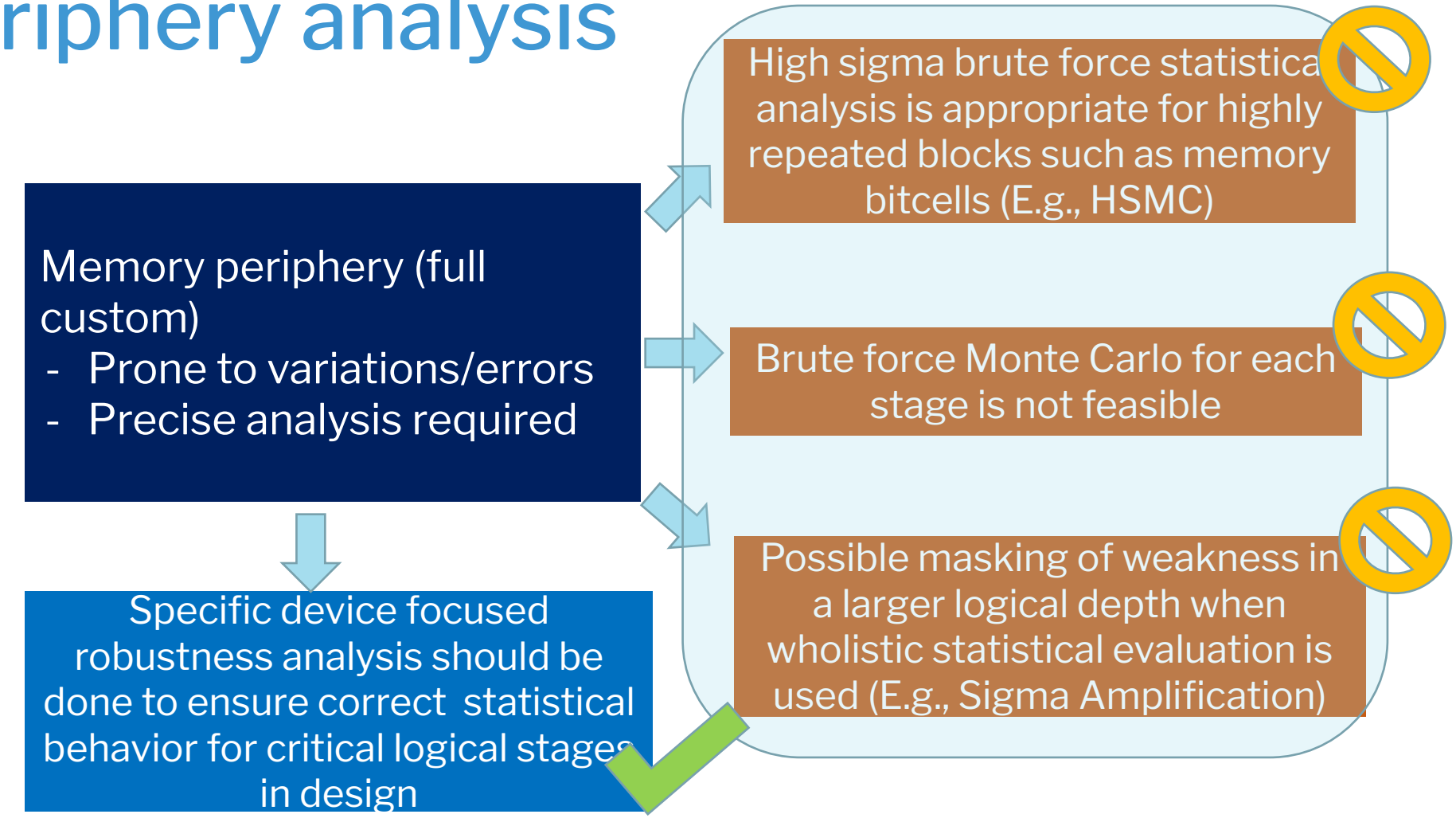
ASICs based on ST proprietary technologies

Possible weaknesses in full custom designed memory periphery

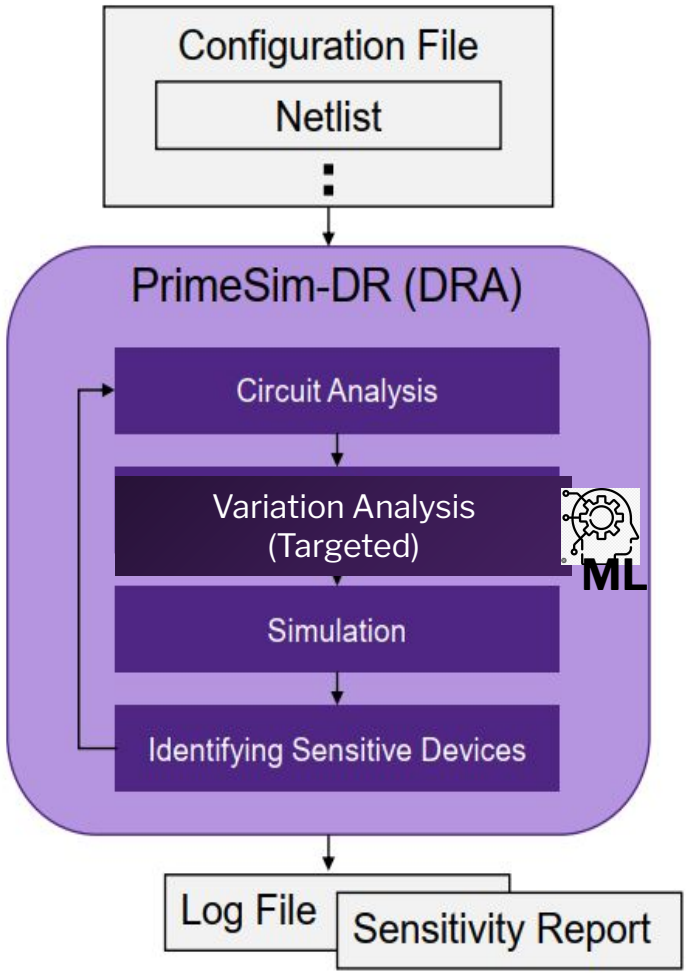


- Memory periphery has many circuits that are hand-crafted and prone to wrong sizing
- This improper sizing can cause design failures
- A design methodology is needed during the design phase to identify and fix such weaknesses

Existing statistical methods and limitations for memory periphery analysis

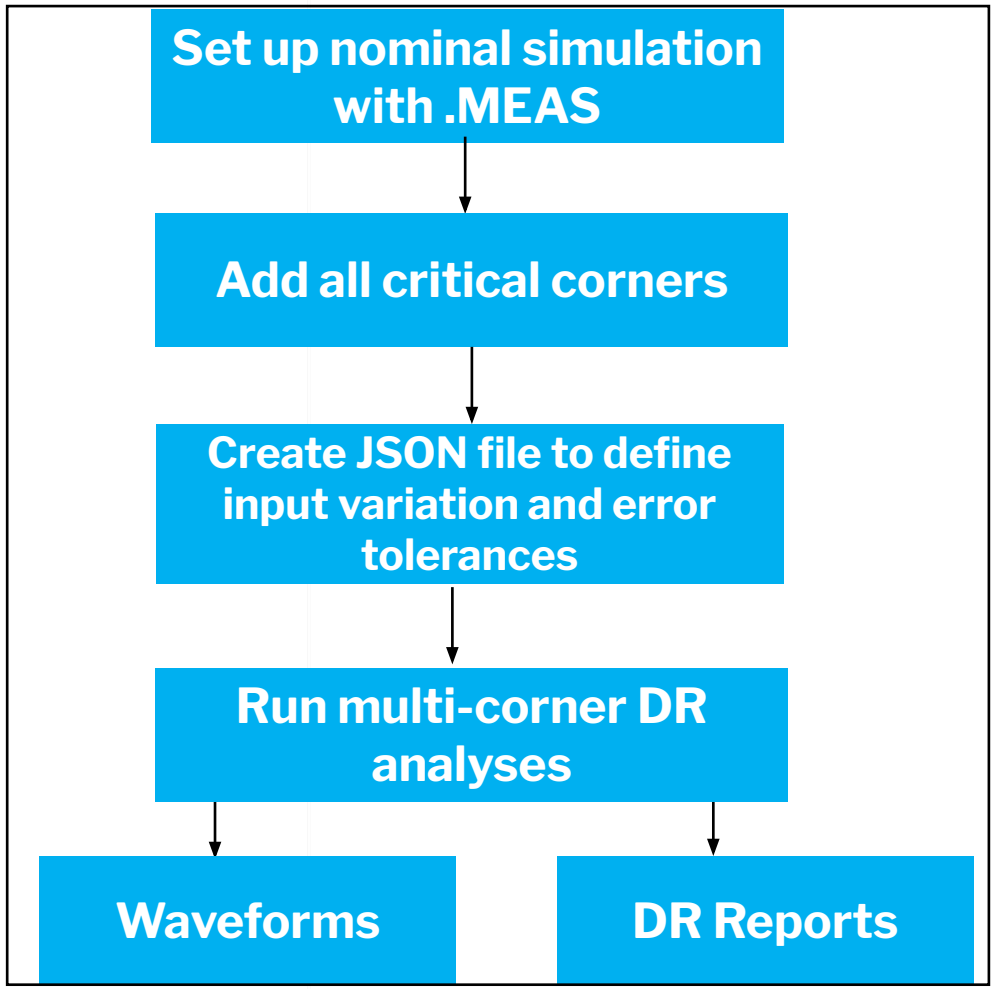


PrimeSim Design Robustness (DR) flow



- Key difference between Monte Carlo methods and DR: DR is applying **variation on one device at a time**
- For a design of 40K **MOSFETs**, variation is introduced in just **~200 MOSFETs** transistors in the final stage to identify the weak devices
- Device features are varied on targeted devices and multiple simulations are run to evaluate the impact on variation on critical measurements

Steps to enable DR



Sample JSON file

```
{
    "dp_config" : "~/my_hosts",
    "dp_num"    : 8,
    "sim_setup" :
    {
        "sim_cmd" : "xa -mt 2 s1.0_fs_130.cir"
    },
    "dr_setup" :
    [
        {
            "dr_tag" : "run_dra_error",
            "stage"  : "dra",
            "dra"    :
            {
                "variation_feature"   : "all",
                "variation_direction" : "plus",
                "delta_vth_val"       : 0.150,
                "delta_ids_pct"       : -40,
                "search_method"       : "error_tol"
            },
            "meas"    :
            {
                "meas_list_file" : "key_meas_file2",
                "set_timing_tol_abs"   : 100e-12,
                "set_timing_tol_rel"   : 5,
                "set_voltage_tol_abs" : 0.005,
                "set_voltage_tol_rel" : 5
            },
            "device" :
            {
                "type"   : "all",
                "exclude_device_filter" : "exclude_file.txt"
            },
            "active_device_flow" : [
            {
                "enable" : true,
                "cck_soa_val_id" : 1e-6,
                "cck_soa_val_ig" : 1e-6,
                "cck_soa_val_is" : 1e-6,
                "cck_soa_val_ib" : 1e-6
            } ]
        }]}
```

Here, we are increasing VTH by 150mV and decreasing IDSAT by 40%
(ΔVth=+150mV, ΔIdsat=-40%)

Specify variation on VTH/IDSAT

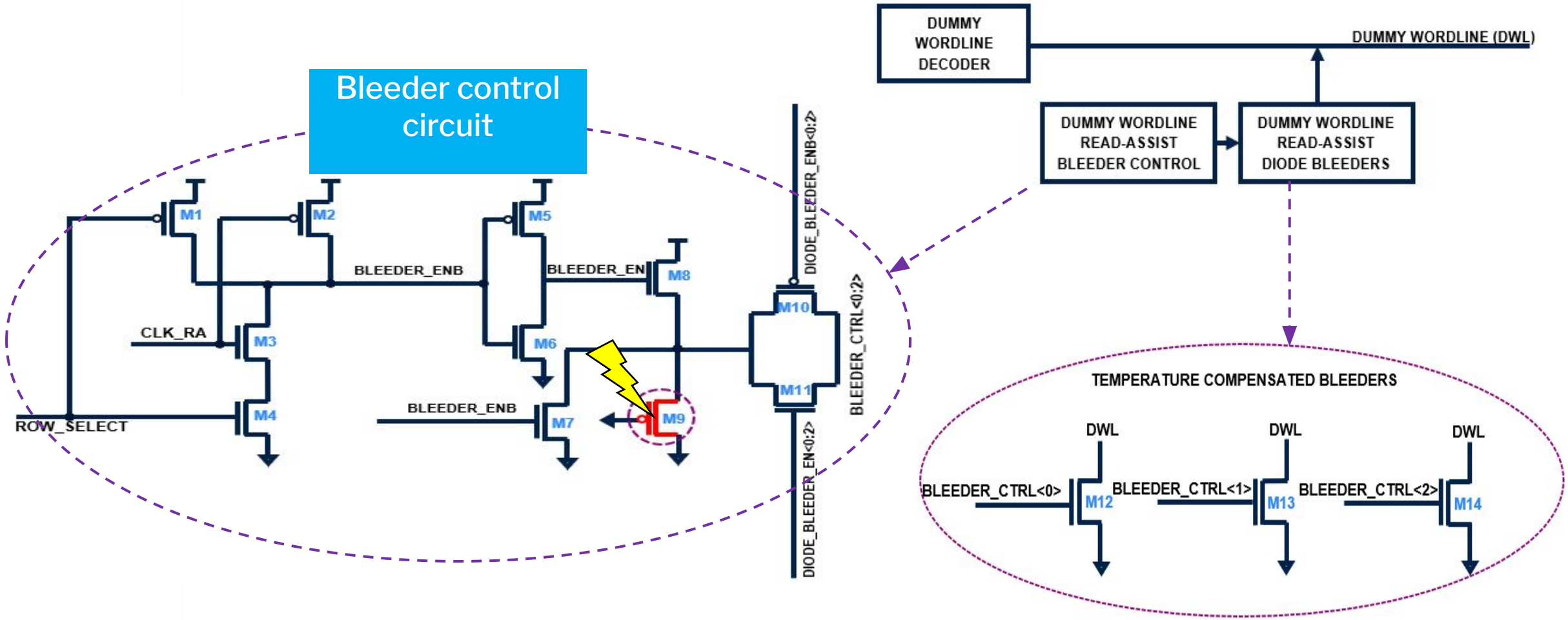
Specify error tolerances

Specify devices to exclude or include

Specify conditions for active device identification

Analysis of DR results

Analysis run on full memory instance – 16384 words x80 bits



US20170301396A1

Analysis of DR results

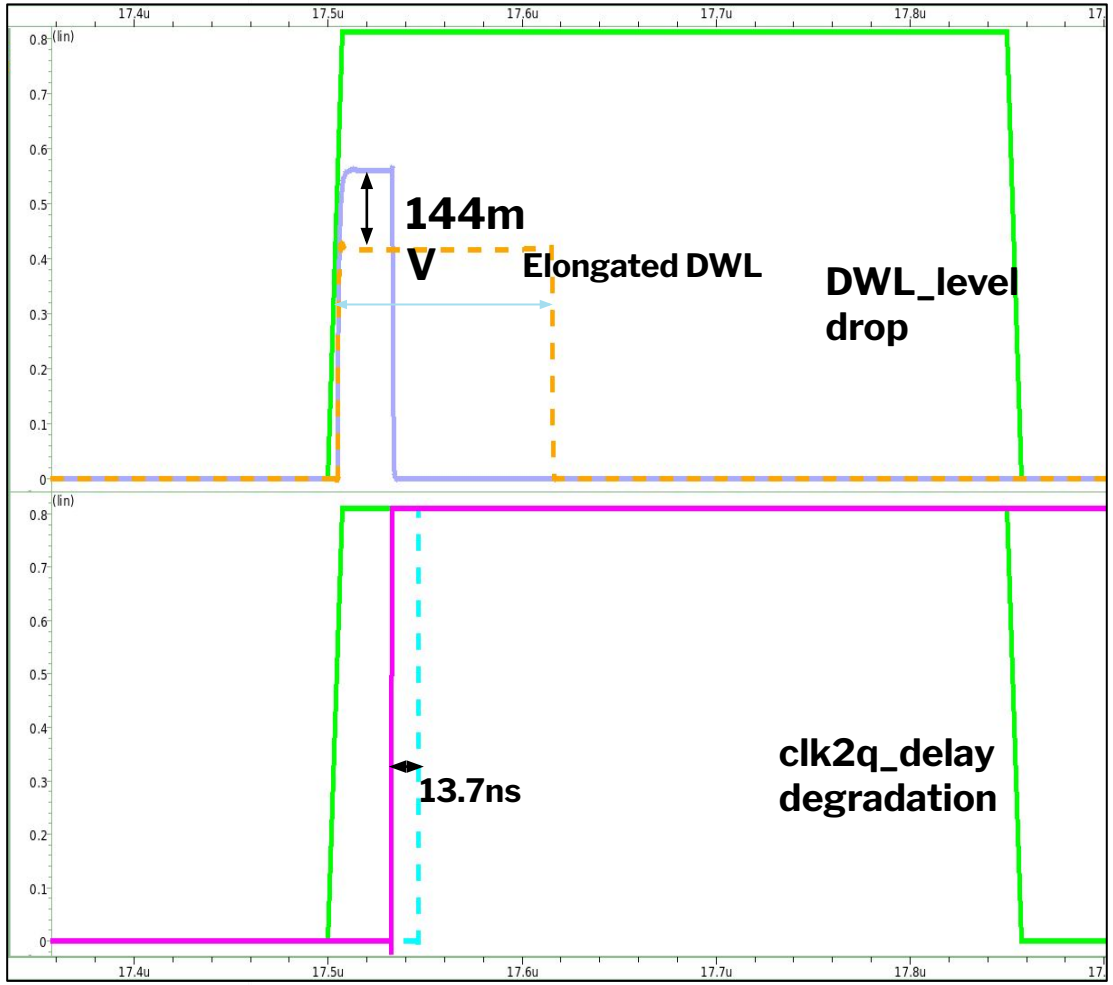
DR Report

```
*,,,,,,
* PRIMESIM_DR linux64 U-2023.03-BETA-20221211,,,,,,
* Build id: 7937803,,,,,,
*,,,,,,
Device_Name,Measurement_Name,Nominal_Result,Variation_Result,Error,Rel_Error(%),Note
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xxidummy_red_ra_mmp_diode:xm:m1,clk2q_delay,2.90674e-08,4.2788e-08,1.37e-08,47.2,
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xmm5:xm:m1,clk2q_delay,2.90674e-08,4.19698e-08,1.29e-08,44.38,
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xxidummy_red_ra_mm6:xm:m1,clk2q_delay,2.90674e-08,1.70454e-08,1.2e-08,41.35,
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xxidummy_red_ra_mmdiode_bleeder0:xm:m1,clk2q_delay,2.90674e-08,1.81248e-08,1.09e-08,37.6
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xxidummy_red_ra_mmdiode_bleeder1:xm:m1,clk2q_delay,2.90674e-08,1.82e-08,1.09e-08,37.38,
xitop:xibotbanks_add0:xidecoder_add0:xirowdecx4_bot:xxirowdec_add0_0_mm5:xm:m1,wl_level,0.674721,0.617991,0.0567,8.4,
xitop:xibotbanks_add0:xidecoder_add0:xirowdecx4_bot:xxirowdec_add0_0_mm5_2:xm:m1,wl_level,0.674721,0.61999,0.0547,8.11,
xitop:xibotbanks_add0:xidecoder_add0:xirowdecx4_bot:xxirowdec_ra_mm6:xm:m1,wl_level,0.674721,0.7252,0.0505,7.48,
xitop:xibotbanks_add0:xidecoder_add0:xirowdecx4_bot:xxirowdec_add0_0_mm5_3:xm:m1,wl_level,0.674721,0.627982,0.0467,6.92,
```

- Above, we see clk2q_delay measurement varying by 47% just because of a single weakened MOS
- Degraded waveforms as a result of device weakening is shown in the next slide
- Identifying such devices is the goal of DR!

Analysis of DR results

Waveform degradation



Dummy Wordline level is deteriorating significantly **(144mV)** under DR (ΔVth=+150mV, ΔIdsat=-40%) impacting the parameter under evaluation (clk2q_delay)

CK
$^{\alpha}$DWL_NOMINAL
$^{\beta}$DWL_DR
$^{\alpha}$Q_NOMINAL
$^{\beta}$Q_DR

α □ _NOMINAL denotes to the nominal simulation without DR induced weakness
β □ _DR refers to the nominal simulation with DR induced weakness

Analysis of DR results

Rerunning DR after fixing the weak device

```
*,,,,,,
* PRIMESIM_DR linux64 U-2023.03-BETA-20221211,,,,,,
* Build id: 7937803,,,,,,
*,,,,,,
Device_Name,Measurement_Name,Nominal_Result,Variation_Result,Error,Rel_Error(%),Note
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xmm5:xm:m1,clk2q_delay,2.07908e-08,4.19025e-08,2.11e-08,101.54,
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xxidummy_red_ra_mm6:xm:m1,clk2q_delay,2.07908e-08,1.57879e-08,5e-09,24.06,
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xxidummy_red_ra_mmdiode_bleeder1:xm:m1,clk2q_delay,2.07908e-08,1.62802e-08,4.51e-09,21.69,
xitop:xibotbanks_add0:xidecoder_add0:xidummy_rowdec_red:xxidummy_red_ra_mmdiode_bleeder0:xm:m1,clk2q_delay,2.07908e-08,1.63051e-08,4.49e-09,21.57,
xitop:xibotbanks_add0:xidecoder_add0:xirowdecx4_bot:xxirowdec_add0_0_mm5:xm:m1,wl_level,0.67472,0.618148,0.0566,8.38,
xitop:xibotbanks_add0:xidecoder_add0:xirowdecx4_bot:xxirowdec_add0_0_mm5_2:xm:m1,wl_level,0.67472,0.620283,0.0544,8.06,
xitop:xibotbanks_add0:xidecoder_add0:xirowdecx4_bot:xxirowdec_ra_mm6:xm:m1,wl_level,0.67472,0.726095,0.0514,7.61,
xitop:xigctrl:xgctrl_red:xxi396_xiclk_gen_xi137_mmn:xm:m1,clk2q_delay,2.07908e-08,2.22255e-08,1.43e-09,6.9,
xitop:xibotbanks_add0:xidecoder_add0:xirowdecx4_bot:xxirowdec_add0_0_mm5_3:xm:m1,wl_level,0.67472,0.629996,0.0447,6.62,
```

- The size of the PMOS in the bleeder control circuit (identified by DR as a weak device) was fixed by resizing
- DR was rerun with this netlist change
- The device disappears from the weak device list
- Bleeder CTRL circuit was verified with corrected sizing. **DWL under-drive sigma reduced from 13mV □ 6.6mV**

Summary and conclusions

- Synopsys PrimeSim™ Design Robustness **identifies weak devices** in large full-custom IPs
- DR Methodology **25X faster** than any other Monte Carlo based method
- DR methodology helps to analyze weakness in design as well as **identifies causes**
- Once the device is identified, **we can resize the device and rerun DR** to validate that the problem is fixed

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Thank You